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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/777,710	02/11/2004	Klaus J. Oberlaender	14303.0068	5914

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EXAMINER	
THAI, TUAN V	

ART UNIT	PAPER NUMBER
2186	

MAIL DATE	DELIVERY MODE
07/26/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/777,710	OBERLAENDER, KLAUS J.	
	Examiner	Art Unit	
	Tuan V. Thai	2186	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *07 December 2006*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-24* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-24* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *11 February 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

Part III DETAILED ACTION

Response to Amendment

1. This office action is in response to Applicant's communication filed December 07, 2006. This amendment has been entered and carefully considered. Claims 1-24 are again presented for examination.

2. Applicant's arguments have been considered but are not deemed to be persuasive. The rejections are maintained as follow.

Claim Rejections - 35 USC § 102

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. § 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless --

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

4. Claims 1-8, 10-14 and 19-21 are rejected under 35 U.S.C. § 102(b) as being anticipated by William et al. (USPN:

5,530,837); hereinafter William.

As per claims 1 and 13; William discloses method for operating a cache memory wherein cache unit comprising a first memory tower/bank, having a first way sub-tower and a second way sub-tower (e.g. see column 1, lines 33 et seq.); a second memory tower, having a first way sub-tower and a second way sub-tower (e.g. see column 1, lines 33 et seq.); and wherein a first cache line of the cache unit includes a first plurality of data segments in the first way sub-tower of the first memory tower and a second plurality of data segments in the first way sub-tower of the second memory tower (similarly for the strings of alternatively storing transactions of data segments in the first and second tower/bank) is equivalently taught as interleaving architecture; (e.g. see column 1, lines 9 et seq.).

As per claim 2, William discloses wherein the first cache line comprises sequential data segments; the first plurality of data segments includes a first data segment and a third data segment; and the second plurality of data segments includes a second data segment and a fourth data segment (e.g. see column 1, lines 25-27);.

As per claim 3, the further limitation of wherein a second cache line of the cache unit includes a first plurality of data segments in the second way sub-tower of the first memory tower and a second plurality of data segments in the second way sub-

tower of the second memory tower is taught by William through the implementation of interleaved architecture (e.g. see column 2, lines 55 et seq.; column 7, lines 50 et seq.);

As per claims 4 and 14; Williams discloses activating first and second memory banks and wherein a physical line of the first memory tower includes data segments from the first cache line and the second cache line (e.g. see column 8, lines 55 et seq.);

As per claims 5 and 6, further comprising a first way multiplexer having a first input port coupled to the first way sub-tower of the first memory tower, a second input port coupled to the first way sub-tower of the first memory port; and an output port; and a second way multiplexer having a first input port coupled to the first way sub-tower of the second memory tower, a second input port coupled to the first way sub-tower of the second memory port and an output port (e.g. see figure 7, column 10, lines 51 et seq.);

As per claims 7 and 8, Williams discloses a tag unit (address select unit 350) coupled to control the first way multiplexer and the second way multiplexer (e.g. see figure 7); and configured to determine whether a memory address is cached by the cache unit (e.g. see column 1, lines 50 et seq.);

As per claim 10, Williams discloses the memory bank of his system comprises multiple blocks or way sub-towers as being claimed which included a third way sub-tower and a fourth way

sub-tower (e.g. see column 8, lines 2 et seq.);

As per claim 11, William discloses his cache system further comprises third memory tower/bank and a fourth memory tower/bank (e.g. see figure 2);

As per claim 12, the further limitation of wherein the first cache line includes a third plurality of data segments in the third memory tower and a fourth plurality of data segments in the fourth memory tower is equivalently taught by Williams as "low-order" and "high-order" interleaving architecture (e.g. see column 2, lines 14 et seq.).

As per claim 19, it encompasses the same scope of invention as to that of claims 1 and 13, the claim is therefore rejected for the same reasons as being set forth above.

As per claim 20, it encompasses the same scope of invention as to that of claims 2 and 14, the claim is therefore rejected for the same reasons as being set forth above.

Allowable subject matter

5. Claims 9, 15 and 21 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and intervening claims. The prior arts of record do not teach nor disclose a data aligner coupled to the output port of the first way multiplexer and the output port of the second way

multiplexer, and the first physical line of the first memory tower has different address than the second physical line of the second memory tower. Claims 16-18 and 22-24 are also objected to since they depended upon the indicated-objectable claims 15 and 21 respectively.

6. As to the remark; Applicant's counsel argue that Williams does not teach a memory tower, which has a first way sub-tower and a second way sub-tower, as required by the claimed invention. Rather, Williams teaches simple memory banks 31, 32. Since Williams does not teach the claimed memory tower, it necessarily follows that Williams can not teach a first cache line with a first plurality of data segments in a first way sub-tower of a first memory tower and a second plurality of data segments in a first way sub-tower of a second memory tower, as required by the claimed invention. Thus the claims are patentable over Williams for at least this reason (amendment, page 11, last paragraphs bridging first paragraph, page 12 et seq.).

With respect to (a); Examiner would like to emphasize that the overall concept of interleaving architecture is clearly taught by Williams wherein the memory tower with the sub-tower structure is well taught and being equivalent to the group of banks and sub-bank as being disclosed and taught by William; for example, William teaches that in figure 2, column 5, lines 7 et

seq. wherein the memory is constructed as an array architecture having multiple groups of banks/towers, wherein the memory address space is partitioned into a number of groups, each group maps into a unique address range and has a plurality of physical memory banks associated with it (e.g. see figure 2). Noting that the physical banks are numbered 0-6, and the starting address for a given bank is indicated at the upper left corner of the bank. Group 0 (tower) is associated with physical banks 0-3 and address range 0 to (X-1); group 1 is associated with banks 4-5 and address range X to (Y-1); and group 2 is associated with bank 6 and address range Y to (Z-1).

7. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 C.F.R. 1.136(a).

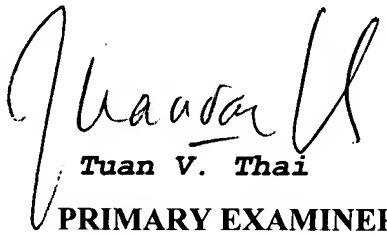
A SHORTENED STATUTORY PERIOD FOR RESPONSE TO THIS FINAL ACTION IS SET TO EXPIRE THREE MONTHS FROM THE DATE OF THIS ACTION. IN THE EVENT A FIRST RESPONSE IS FILED WITHIN TWO MONTHS OF THE MAILING DATE OF THIS FINAL ACTION AND THE ADVISORY ACTION IS NOT MAILED UNTIL AFTER THE END OF THE THREE-MONTH SHORTENED STATUTORY PERIOD, THEN THE SHORTENED STATUTORY PERIOD WILL EXPIRE ON THE DATE THE ADVISORY ACTION IS MAILED, AND ANY EXTENSION FEE PURSUANT TO 37 C.F.R. § 1.136(a) WILL BE CALCULATED FROM THE MAILING DATE OF THE ADVISORY ACTION. IN NO EVENT WILL THE STATUTORY PERIOD FOR RESPONSE EXPIRE LATER THAN SIX MONTHS FROM THE DATE OF THIS FINAL ACTION.

8. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Tuan V. Thai whose telephone number is (571)-272-4187. The examiner can normally be reached on from 6:30 A.M. to 3:00 P.M..

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mathew M. Kim can be reached on (571)-272-4182. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see ***http://pair-direct.uspto.gov***. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

TVT/July 20, 2007



Tuan V. Thai
PRIMARY EXAMINER
Group 2100